IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 06-788 (JJF)
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S
FOURTH NOTICE OF 30(b)(6) DEPOSITION
OF DEFENDANT FREESCALE SEMICONDUCTOR, INC.

PLEASE TAKE NOTICE that pursuant to Rules 26 and 30 of the Federal Rules of Civil Procedure, plaintiff ProMOS Technologies, Inc. will take the deposition of defendant Freescale Semiconductor, Inc. ("Freescale"), through its corporate designee(s), before a person authorized to administer an oath at the offices of Ashby & Geddes, 500 Delaware Avenue, 8th Floor, Wilmington DE 19899, commencing at 9:30 a.m. on January 14, 2007, or at such other date and time as counsel for the parties shall agree, and continuing from day to day until completed. The deposition may be recorded by audio-visual means as well as stenographically.

Pursuant to Rule 30(b)(6) of the Federal Rules of Civil Procedure, Freescale shall designate one or more officers, directors or managing agents, or other persons who consent to testify on its behalf concerning the subjects identified in Attachment A, and if more than one person is so named, designate for each person the subject or subjects on which that person will testify.

ASHBY & GEDDES

/s/ *Lauren E. Maguire*

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Dated: December 21, 2007
186851.1

ATTACHMENT A

1. The manufacturing process flows, process recipes, and any other process information for any products manufactured during the period January 1, 2004 to the present using any variation of HiP 7 and/or HiP 8, including their identity and content.

2. The manufacturing process flows, process recipes, and any other process information for any products manufactured during the time period January 1, 2004 to the present (other than the HiP7 and HiP8 flows identified in Topic No. 1), including but not limited to all processes identified in Exhibit 6 to the Scott Bolton Deposition ("Bolton Exhibit No. 6"), including their identity and content.

3. The identification of any Freescale manufacturing process on which Freescale intends to rely for any invalidity defense.

4. The manufacturing process flows, process recipes, and any other process information for any processes identified in response to Topic No. 3 above, including their identity and content.

5. Separately for each process identified in Bolton Exhibit No. 6, the identification of each product that is manufactured using each such process.

6. Code names, project designations, product families, part numbers and any other naming or grouping conventions used for any product manufactured using any of the processes identified in Bolton Exhibit 6.

7. With respect to each process covered by topics 1-4 above, the process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride.

8. The similarities and differences among the processes used to manufacture Freescale products from December 2000 to the present, including the similarities and differences among the process flows, process recipes, and other process information.

9. The similarities and differences among the various HiP7 processes used to manufacture Freescale products, including the similarities and differences among the process flows, process recipes, and other process information.

10. The similarities and differences among the various HiP8 processes used to manufacture Freescale products, including the similarities and differences among the process flows, process recipes, and other process information.

11. With respect to each process covered by topics 1-4 above, any testing, imaging or analysis performed by or on behalf of Freescale that relates to any changes in the physical structure of the device as a result of the RF Preclean step prior to the deposition of the Ti glue layer and/or TiN barrier layer during the qualification process or the manufacturing of Freescale products.

12. With respect to each process covered by topics 1-4 above, Freescale's efforts to test or characterize the occurrence of volcanoes and/or voids in the tungsten layer during the qualification process or in manufacturing products.

13. With respect to each process covered by topics 1-4 above, Freescale's efforts to measure the resistance of the tungsten based interconnect, both during the qualification of the process and during the manufacture of products.

14. With respect to each process covered by topics 1-4 above, any thickness measurement data, procedures for making those measurements and the specification of the allowed thickness range of the titanium adhesion layer and the titanium nitride barrier layer.

15. With respect to each process covered by topics 1-4 above, the temperatures and duration of the rapid thermal anneal sequence used after the deposition of the TiN layer.

16. With respect to each process covered by topics 1-4 above, Freescale's efforts to characterize the microstructure, such as the grain size and the crystallographic texture, of the TiN layer both before and after the nitrogen plasma treatment step.

17. With respect to each process covered by topics 1-4 above, Freescale's efforts to measure the resistance of the TiN layer both before and after the nitrogen plasma treatment step.

18. With respect to each process covered by topics 1-4 above, the mechanism whereby precursor or source materials used for the deposition of the TiN layer are released into the vapor phase in the deposition chamber.

19. With respect to each process covered by topics 1-4 above, the implementation or qualification of the GLU-APOLLO process/recipe, including but not limited to any performance comparison tests with the previous process of record.

20. With respect to each process covered by topics 1-4 above, the design rules for products manufactured using each such process, including but not limited to the length and depth of any tungsten metal lines made with a damascene or dual-damascene process, as well as the identity of the circuit elements in electrical contact with the tungsten metallization through the Ti/TiN glue/barrier layer.

21. With respect to each process covered by topics 1-4 above, the date of first use of the process, the date of first public use of the process, and the date of first sale of any product manufactured using that process.

22. Freescale's efforts to change or modify any process to design around the Fortin patent, including all communications relating to such efforts.

23. The types and locations of documents relevant to each of the foregoing topics.